EE 330
Homework 6
Fall 2022 (This assignment is due Friday Sept 30 at 1:00 PM)

Assume a CMOS process is characterized by model parameters extracted from an ON 0.5µm appended below.

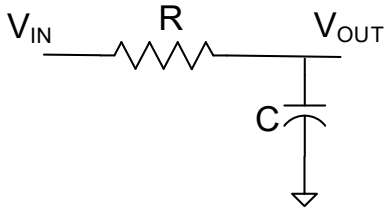
Problem 1 Assume a resistor has a resistance of 1KΩ at T=300°K. If the TCR of this resistor is constant of value 2000 ppm/°C, what will be the resistance at T=350°K?

Problem 2 Consider an n+ diffused resistor that is 200u long, 1.5u wide, and 2u thick. What is the nominal value of the resistance if it is doped with Phosphorus and the doping density is uniform 5E14/cm^3.

Problem 3 Consider a 10K resistor that is made by the series connection of two resistors. One of the resistors is a n+ doped 3KΩ polysilicon resistor with a TCR of -1200 ppm/°C and the other is a p+ diffused silicon 7KΩ resistor with a TCR of 800 ppm/°C. What is the TCR of the series combination? How does this compare to the TCR that would be achieved if the 10K resistor were made entirely with n+ doped polysilicon?

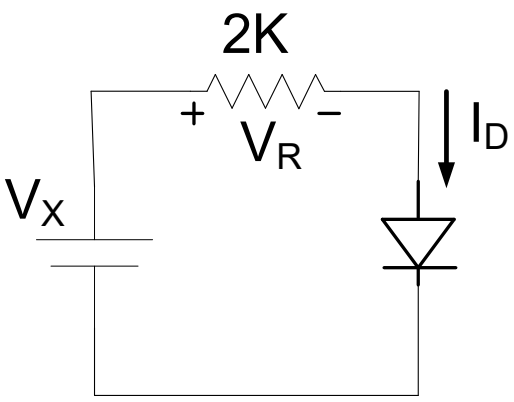
Problem 4 Consider the first-order lowpass filter (LPF) shown below that has a 3dB frequency of 10MHz when operating at T=273°K. Assume the resistor has a value of 10KΩ at this operating temperature.

a) If the TCR of this resistor is constant of value 2300 ppm/°C and the capacitor has a constant TCC of 1000 ppm/°C, plot the frequency response for the LPF at T=273°K and T=350°K.
b) What percent change occurs in the 3dB frequency when the temperature is increased from T=273°K to T=350°K. Assume the temperature coefficients used in part a)



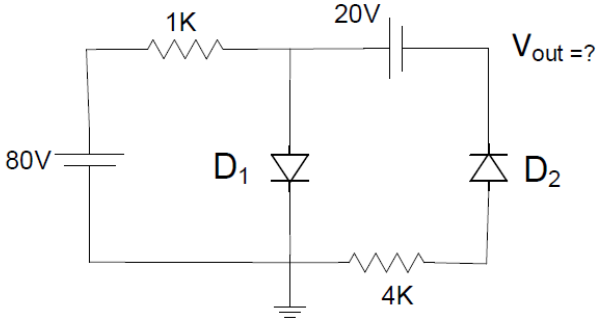
Problem 5 If the voltage of a forward-biased pn junction is varied between 0.5V and 0.6V, what is the range in the diode current. Assume the junction area of the diode is 50µ^2 and $J_S=10^{-15}$A/µ^2.

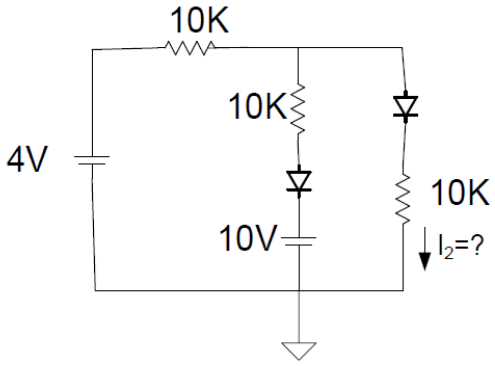
Problem 6 Determine the current I_D (within ±5%) if V_X=10V for the following circuit. Assume the area of the diode is 200µ^2 and $J_S=10^{-15}$A/u^2.



Problem 7 Repeat Problem 6 if V_X=520mV.

Problem 8 Determine the quantities indicated with a ? in the following circuits. Assume the diodes are ideal.





Problem 9 and 10 Implement a 4 to 1 multiplexer and a 1 to 4 demultiplexer, both with an active low enable pin, using Verilog. When the multiplexer/demultiplexer is disabled, its output should be low. Design a testbench proving function using Verilog. Submit module code, testbench code, and Modelsim waveforms.

Passive Process Parameters for ON 0.5µm CMOS Process											
	N+	P+	POLY	POLY2	HR_P2	M1	M2	M3	N/PLY	N_W	UNITS
RESISTANCES											
Sheet Resistance	84	105	23.5	999	44	0.09	0.10	0.05	825	815	Ohms/sq
Contact Resistance	65	150	17		29		0.97	0.79			Ohms
CAPACITANCES											
Area (substrate)	425	731	84			27	12	7		37	af/µm^2
Area (N+ active)			2434			35	16	11			af/µm^2
Area (P+active)			2335								af/µm^2
Area (POLY)				938		56	15	9			af/µm^2
Area (POLY2)						49					af/µm^2
Area (metal 1)							31	13			af/µm^2
Area (metal 2)								35			af/µm^2
Fringe (substrate)	344	238				49	33	23			af/µm
Fringe (poly)						59	38	28			af/µm
Fringe (metal 1)							51	34			af/µm
Fringe (metal 2)								52			af/µm
Overlap (N+active)			232								af/µm
Overlap (P+active)			312								af/µm